Abstract of the Disclosure

A dielectric memory cell comprises a substrate which includes a source region, a drain region, and a channel region positioned there between. A multilevel charge trapping dielectric is positioned on the surface of the substrate and a control gate is positioned on the surface of the dielectric and is positioned over and aligned with the channel region. The multilevel charge trapping dielectric includes a tunneling dielectric layer, a charge trapping dielectric layer, and a top dielectric layer. The tunneling dielectric layer comprises a first dielectric material having a wide band gap between a tunneling dielectric layer valance band Fermi level and a tunneling dielectric layer conduction band Fermi level. The top dielectric layer comprises a second dielectric material having a valance band Fermi level approximately equal to the tunneling dielectric layer valance band Fermi level and having a conduction band Fermi level greater than the tunneling dielectric layer conduction band Fermi level. The charge trapping layer is positioned between the bottom layer and the top layer of a third dielectric with charge trapping properties.